IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors:	Chian-Min Richard Ho et al.
Assignee:	0IN Design Automation, Inc.
Title:	Method for automatically searching for defects in a description of a circuit

Serial No.:	09/849,005	Filing Date:	May 4, 2001
Examiner:	Frejd, Russell Warren	Group Art Unit:	2123
Docket No.:	0IN006-1C US	Confirmation No:	1848

Santa Clara, California
October 10, 2003

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA VA 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.97(c)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, §1.97 and §1.98, the Applicants submit for consideration in the above-identified patent application the documents listed on the accompanying Forms PTO-1449. The Forms PTO-1449 are submitted in two parts, namely Part A of 3 sheets and Part B of 24 sheets. Copies of 28 documents cited in Part A are also submitted herewith (but references 9, 10 and 11 are not being submitted and the Examiner is requested to obtain them from the USPTO files of the parent application). The Examiner is requested to make all these documents of record. Applicants would appreciate the Examiner initialing and returning the all the Forms PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement is submitted pursuant to 37 CFR §1.97(c) as it is after receipt of a first Office Action on the merits but before mailing of a final Action or Notice of Allowance. Accordingly, a fee is required pursuant to 37 CFR §1.17(p). A Fee Transmittal form (PTO/SB/17) is attached to this submission.

In addition, Applicants submit for the Examiner's consideration the following list of co-owned patents and application, cited by serial number, first named inventor and

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filing date. The Applicants presume that the Examiner has access to and will review the co-owned patents and applications and the files thereof for any office actions, amendments or other materials that may be relevant to the patentability of the claims of the present application. For any such U.S. patent application(s) that are currently pending, the Applicants further presume that the Examiner will consider any future office actions, amendments or other materials in the file thereof that may be relevant to the patentability of the claims herein. **If the Applicants' understanding in this regard is not correct, please notify the undersigned so that copies of any such documents can be submitted to the Examiner**

	Serial No.:	First Named Inventor	Filing Date:
1.	08/955,329	Ly et al.	10/20/1997
2.	09/635,598	Ly et al.	8/9/2000
3.	10/348,116	Ly et al.	1/20/2003
4.	08/954,765	Ho et al.	10/20/1997

The information contained in this Information Disclosure Statement under is to the best of my knowledge and is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.
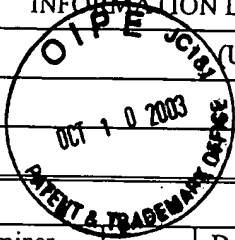
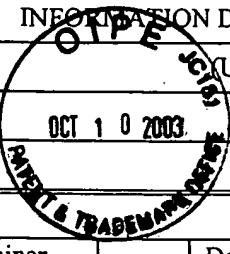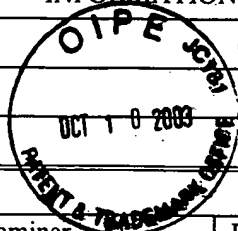| **Via Express Mail Label No.** **ER 205 704 792 US**	Respectfully submitted,

Respectfully submitted,

S. Omkar

Omkar K. Suryadevara
Attorney for Applicants
Reg. No. 36,320

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	AB	5,630,051	5/13/97	Sun et al.	395	183.08	
	AC	5,600,787	2/4/97	Underwood et al.	395	183.06	
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	AJ	Clarke, E. M., et al., "Efficient Generation of Counterexamples and Witnesses in Symbolic Model Checking", 32nd Design Automation Conference, June 12-16, 1995, pp. 427-432.
	AK	Silburt, Allan, et al., "Accelerating Concurrent Hardware Design with Behavioral Modelling and System Simulation", 32nd Design Automation Conference, June 12-16, 1995, pp. 528-533.
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	AM	Clarke, Edmund M., et al., "Model Checking and Abstraction", ACM Press Conference Record of the Nineteenth Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, January 19-22, 1992, pp. 343-354.
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	AO	Clarke, E. M., "Representing Circuits More Efficiently in Symbolic Model Checking", 28th ACM/IEEE Design Automation Conference, June 17-21, 1991, pp. 403-407.

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	AI	Bombana, M., et al., "Design-Flow and Synthesis for ASICs: a case study", 32nd Design Automation Conference, June 12-16, 1995, pp. 292-297.
	AJ	Beer, Ilan, et al., "Methodology and System for Practical Formal Verification of Reactive Hardware", 6th International Conference, CAV '94, June 21-23, 1994, Proceedings, pp. 183-193.
	AK	Daga, A., "A Symbolic-Simulation Approach to the Timing Verification of Interacting FSMs", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, 584-589.
	AL	Matsunaga, Y., "An Efficient Equivalence Checker for Combinational Circuits", 33rd Design Automation Conference, Las Vegas, NV, 1996 Proceedings, pp. 629-634.
	AM	Balarin, F. , et al., "Formal Verification of Embedded Systems based on CFSM Networks", 33rd Design Automation Conference, Las Vegas, NV, 1996, 568-571.
	AN	Stornetta, T., et al., "Implementation of an Efficient Parallel BDD Package", 33rd Design Automation Conference, Las Vegas, NV, 1996, 641-644.
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	AJ	Groz, R., et al. "Attacking A Complex Distributed Algorithm from Different Sides: An Experience with Complementary Validation Tools", Proc. IFIP WG 6.1 Fourth International Workshop on Protocol Specification, Testing and Verification, Skytop Lodge, Pennsylvania, June 1984, pp. 315-331.
	AK	Nurie, G. "Attain Testability With Hierarchical Design", Electronic Design, June 27, 1991, pp. 89-99.
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	AM	Ho, Chian-Min Richard, "Validation Tools For Complex Digital Designs", A Dissertation Submitted to the Department of Computer Science and the Committee on Graduate Studies of Stanford University in Partial Fulfillment of the Requirements For the Degree of Doctor of Philosophy, November 1996.
	AN	Von Bochmann, G., "Concepts for Distributed Design", Springer-Verlag Berlin Heidelbeg New York, 1983.
	AO	Torku, K. E., "Fault Test Generation for Sequential Circuits: A Search Directing Heuristic", Ph.D. Thesis, University of Oklahoma, 1979.

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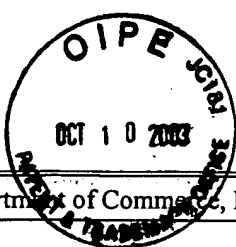
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	AJ	http:www.parasoft.com, "Insure++ Getting Started Version 3.0.1", believed to be prior to October 1997..
	AK	Huey, B. M., "Search Directing Heuristics for the Sequential Circuit Test Search System (SCIRTSS)", Ph.D. Thesis, University of Arizona, 1975.
	AL	Deutsch, M. S., "Software Verification and Validation", Prentice-Hall, Englewood Cliffs, NJ, 1982.
	AM	Masud, M., et al., "Functional Test Using Behavior Models", Digest of Papers COMPCON Spring 1992, San Francisco, CA February 1992, pp. 446-451.
	AN	Brayton, R. K., et al., "VIS" First International Conference Formal Methods in Computer Aided Design, FMCAD'96, Palo Alto, CA, November 1996, pp. 248-256.
	AO	Chandra, A. K., et al., "Architectural Verification of Processors Using Symbolic Instruction Graphs", Computer Science, February 9, 1994, pp. 1-23.

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	AI	Burch, Jerry R., et al., "Automatic Verification of Pipelined Microprocessor Control", Computer Aided Verification, 6th International Conference, CAV'94, Stanford, CA, June 21-23, 1994 Proceedings, pp. 69-80.
	AJ	Malley, Charles, et al., "Logic Verification Methodology for Power PC™ Microprocessors", 32nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 234-240.
	AK	Campos, S., et al., "Verifying the Performance of the PCI Local Bus using Symbolic Techniques", International Conference on Computer Design: VLSI in Computers & Processors, October 2-4, 1995, Austin, Texas, pp. 72-78.
	AL	http://www.synopsys.com/pubs/JHLD/JHLD-099402, System Design and Validation, believed to be prior to October 1997.
	AM	Beatty, Derek L., "Formally verifying a microprocessor using a simulation methodology", 31st Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 596-602.
	AN	Beer, Ilan, et al., "Rule-Base: an Industry-Oriented Formal Verification Tool", 33rd Design Automation Conference, Proceedings 1996, 655-660.
	AO	Bormann, Jorg, et al., "Model Checking in Industrial Hardware Design", 32nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 298-303.

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	AJ	Mihail, Milena, et al., "On the Random Walk Method for Protocol Testing", Computer Aided Verification, 6th International Conference, CAV '94, Stanford, CA, June 21-23, 1994, pp. 133-141.
	AK	Cheng, Kwang-Ting, "Automatic Generation of Functional Vectors Using the Extended Finite State Machine Model", 33rd Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 57-78.
	AL	Ramalingam, T., et al., "On conformance test and fault resolution of protocols based on FSM model", Proceedings of the IFIP TC6 Working Conference on Computer Networks, Architecture and Applications, NETWORKS '92, Trivandrum, India October 28-29, 1992, pp. 211-223.
	AM	Chechik, M., et al., "Automatic Verification of Requirements Implementation", Proc. 1994 International Symposium on Software Testing and Analysis (ISSTA), Seattle, WA, August 1994, pp. 109-124.
	AN	v. Bochmann, G. et al., "Protocol Testing: Review of Methods and Relevance for Software Testing", ACM Press, Proceedings of the 1994 International Symposium on Software Testing and Analysis (ISSTA), Seattle, Washington, August 17-19, 1994.
	AO	Fujiwara, S., et al., "Test Selection Based on Finite State Models", IEEE Transactions on Software Engineering, Vol. 17, No. 6, June 1991, pp. 591-603.

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	AJ	Fuchs, N. E., "Specifications are (preferably) executable", Software Engineering Journal, September 1992, pp. 323-334.
	AK	Narasimhan, Naren, et al., "Specification of Control Flow Properties for Verification of Synthesized VHDL Designs", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96, Palo Alto, CA, November 6-8, 1996, pp. 326-345.
	AL	Keutzer, K., "The Need for Formal Verification in Hardware Design and What Formal Verification Has Note Done for Me Lately", Workshop on the HOL Theorem Proving System and its Application, 1991, pp. 77-86.
	AM	Eiriksson, Asgeir T., "Integrating Formal Verification Methods with A Conventional Project Design Flow", 33rd Design Automation Conference, Las Vegas, NV, Proceedings 1996, pp. 666-671.
	AN	Borrione, D., et al., "HDL-Based Integration of Formal Methods and CAD Tools in the PREVAIL Environment", Formal Methods in Computer-Aided Design, First International Conference, FMCAD '96 Palo Alto, CA, November 6-8, 1996, pp. 451-467.
	AO	Aziz, A., et al., "HSIS: A BDD-Based Environment for Formal Verification", 31st Design Automation Conference, San Diego, CA, June 6-10, 1994, pp. 454-459.

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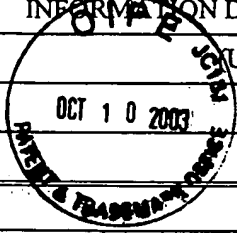
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	AJ	v. Bochman, G., "Usage of Protocol Development Tools: The Results of a Survey", Protocol IFIP WG 6.1, Seventh International Workshop on Protocol Specification, Testing and Verification, 1987, pp. 139-161.
	AK	Borgmann, J., et al., "Model Checking in Industrial Hardware Design", 32nd Design Automation Conference, San Francisco, CA, June 12-16, 1995, pp. 298-303.
	AL	Miczo, A.., "Digital Logic Testing and Simulation", John Wiley & Sons, New York, NY, 1986.
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	AN	Smith, S., et al., "Demand Driven Simulation: BACKSIM", 24th ACM/IEEE Design Automation Conference, Proceedings 1987, pp. 181-187.
	AO	Levitt, J., et al., "A Scalable Format Verification Methodology for Pipelined Microprocessors", 33rd Design Automation Conference, Proceedings 1996, pp. 558-563.

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	AK	Nelson, B. E., et al., "Simulation Event Pattern Checking with PROTO[1]", June 14, 1993.
	AL	Fallah, F., et al., "Functional Vector Generation for HDL models Using Linear Programming and 3-Satisfiability, believed to be prior to October 1997.
	AM	Moundanos, D., "Abstraction Techniques for Validation Coverage Analysis and Test Generation", IEEE Transactions on Computers, Vol. 47, January 1998, pp. 2-14.
	AN	Hsiao, M. S., et al., "Application of Genetically Engineered Finite-State-Machine Sequences to Sequential Circuit ATPG", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 3, March 1998, pp. 239-254.
	AO	Gregory, B., et al., "Method for processing a hardware independent user description to generate logic circuit elements including flip-flops, latches, and three-state buffers and combinations thereof", http://patent.womp.ent number=5661661, believed to be prior to October 1997.

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	AJ	Hastings, R., "Method and apparatus for modifying relocatable object code files and monitoring programs", http://patent.womp...ent_number=5535329, believed to be prior to October 1997.
	AK	Cheng, K. T., "Automatic Functional Test Generation Using The Extended Finite State Machine Model", 30th Design Automation Conference, Dallas, Texas, June 14-18, Proceedings 1993, pp. 86-91.
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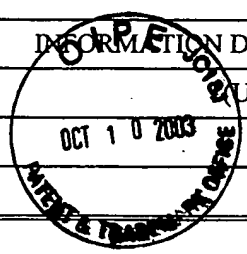
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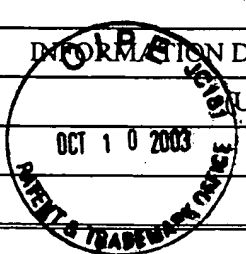
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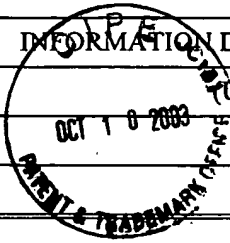
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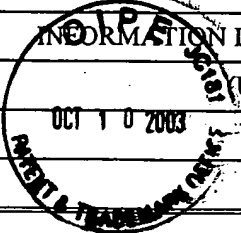
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U.S. Department of Commerce, Patent and Trademark Office		Atty Docket No.		Serial No.	
		01N0064CUS		09/849,005	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Applicants: Chian-Min Ho et al.			
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		Filing Date		Group	
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U.S. Patent Documents

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	AA						
	AB						
	AC						
	AD						
	AE						
	AF						

Foreign Patent Documents

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